

# The design and development of a fault indicator for amplifier circuits

Trudy Sutherland

Vaal University of Technology  
Vanderbijlpark, South Africa

**ABSTRACT:** Faultfinding shortcomings during practical periods have been identified. A solution of how to make faultfinding logic and systematic, to start at the beginning but not to identify the specific fault condition, has to be found. All electronic circuits can be analysed; indeed, it is possible to break down circuits into specific sections. The Fault Indicator Device (FID) has been designed and constructed for second year electronic learners at the Vaal University of Technology, Vanderbijlpark, South Africa. In order to make the FID more economical, three types of amplifier circuits can be tested. The three types are the common emitter (CE), common base (CB) and common collector (CC). A test was conducted on all three types of amplifier circuits, which proved to be successful. A selector switch on the FID allows for amplifier type selection. All of the amplifier circuits can be divided into two sections, limiting the components, and all of the FIL panels identified the fault areas correctly. The tests conducted showed that the section selection is quick and effective, taking only minutes to identify the specific fault within an amplifier circuit thereafter.

## INTRODUCTION

Identifying the lack of skills concerning electronic practical experiments can only occur if a fair amount of time is spent with learners [1]. Basic skills can be incorporated within the theory class; however skills needed to complete the practical experiments are *hands on* skills and learners need a lot of patience and assistance from lecturers to learn these skills. However, this is a time consuming task as the complete circuit has to be analysed.

A specially designed Fault Indicating Device (FID) can carry out partitioning. The Fault Indication Lights (FIL) identify the specific section at the fault. This leads to a better understanding of how faultfinding takes place in a circuit. Faultfinding can be seen as a specific sequence that takes place. After analysing a couple of smaller sections of the major circuit, it becomes clear to the learners what is expected from them during faultfinding.

Once the faulty area is identified via the FIL, learners have to identify all of the components within this section. They need to make sure that all of the connections within this section are correctly executed. Therefore, learners need to understand the basic rules for connecting a circuit on a project board. These theoretical and practical skills have been completed during the first year of studying electronics at the Vaal University of Technology, Vanderbijlpark, South Africa. Once all of the connections are correctly executed, then it becomes time to look at the components that are located within the identified section.

As faultfinding is very time consuming, it definitely saves time by analysing certain smaller sections of a circuit separately. If more than one section is faulty, the learner can repeat all of the faultfinding steps and, with some repetition, be able to master the faultfinding techniques.

## THE PROBLEM STATEMENT

Time is a problem when faultfinding. Lecturers teach with different styles and at different speeds. Not everybody carries out faultfinding during theory periods. Most lecturers still believe it falls under practical periods. This influences the learner's attitude towards practical skills, which are needed desperately in the work environment. If time spent on faultfinding can be reduced, learners are able to address these skill requirements within the work environment. Learners experience less stress when doing practicals and, therefore, learn more.

The purpose of this research is to design and construct an Electronic Fault Indicator Device to test amplifier circuits; this will use individual and interchangeable Light Indicator Device panels to specify a certain area that is at fault for the amplifier circuit being tested.

### Importance of the Study

With the rapid changes in technology, it is important to teach learners the necessary skills that are needed within the contemporary work environment. The demand for a skilled and educated workforce is on the increase [2]. Higher education institutions must be increasingly efficient and effective in providing this value, or else they are at risk of losing their place in the market [3].

Furthermore, education should concentrate more on the increasing demand for new knowledge and skills by focusing on the physical development of the brain, as well as on the ability of a person to utilise the brain by stimulation [4]. All of this places engineering education under tremendous pressure to continue providing quality graduates to their customers – the challenge is how to achieve this [5].

## TEST DEVICES IN USE

The test devices currently in use are not relevant to the FID. No device that analyses electronic amplifier circuits could be found. Those in use are mostly based on Printed Circuit Board (PCB) faultfinding. Characteristics of test devices in use are as follows:

- The system 8 Range can only trace faults if a good PCB's voltages and currents are known [6];
- The Vector Plane Stimulus (VPS) system is only used to identify a short circuit on a PCB [7];
- The CK 100 Logic Probe is mainly utilised in digital applications and gives visual and audio indication of a fault's existence [8];
- The RITS520a system tracks down faults faster than a fixture [9]. However, this system is also applicable to PCBs and is not meant for laboratory amplifier circuits;
- The FT100s system is basically used in the manufacturing and service fields. The system tests PCB faults and requires a functioning PCB for the system to identify the response of the functional board [10].

These faultfinding techniques have been in use for many years. These techniques alone do not seem to be effective with learners and, as such, it becomes necessary to develop an alternative method for faultfinding.

## THE GENERAL LAYOUT

It was decided to test the alternating current (ac) input and the output signals first. If the amplifier circuit under test is correctly built, this test will indicate it via Light Emitting Diodes (LEDs). The lecturer, technician and learner can immediately see that the circuit under test is functioning correctly, as the allocated input and output LEDs show. This is illustrated in Figure 1.

The next step is to test the direct current (dc) voltages of the amplifier circuits under test. All three-amplifier circuits being tested make use of the same dc testing points, which are the dc voltages on the transistors: base, collector and emitter. Figure 2

illustrates the transistor terminals test. The FIL indicates, via LEDs, if there is a fault within the amplifier circuit. If this should be the case, the corresponding LED (section where fault occurs) on the FIL lights up.

## THE INPUT DESIGN LAYOUT

To test if the applied ac input to the amplifier circuit being tested is correct, it must be compared with an ac test signal onboard the FID. Therefore, it is necessary to design, build and test a signal generator. The amplitude and frequency is indicated via two seven-segment Liquid Crystal Displays (LCDs). The learner selects the desired amplitude and frequency (for correlation purposes) on the FID. The onboard signal generator displays three signals, namely a sinusoidal, square and triangular waveform. Even though amplifier circuits only use the sinusoidal waveform, the square output waveform is applied to the tachometer, which drives the frequency LCD. The signal generator design has only a frequency control available. As such, an extra circuit for voltage control is designed (see Figure 3).

To select very small amplitudes from the onboard signal generator, a subtractor attenuator circuit is added. The output of the attenuator is applied to a micro controller. The input signal applied by the learner to the amplifier circuit is also applied to the controller. The controller then compares the two signals amplitude's and frequency. The sampling of frequency and amplitude is necessary, as different signal generators are used and, are usually not synchronised, as is in this case. It is important that the sample determines if the frequency and the voltages correlates with each other. The output of the controller switches the input LED on when the learner's applied signal is correct.

If the input LED is off, the input applied to the amplifier circuit under test is faulty. The learner can immediately compare the applied input signal with the input of the amplifier circuit under test. If the input LED emits, the learner can continue and verify if the output LED is on or off. If the output LED is off, the learner can assume that there is a fault within the constructed amplifier circuit on the project board.

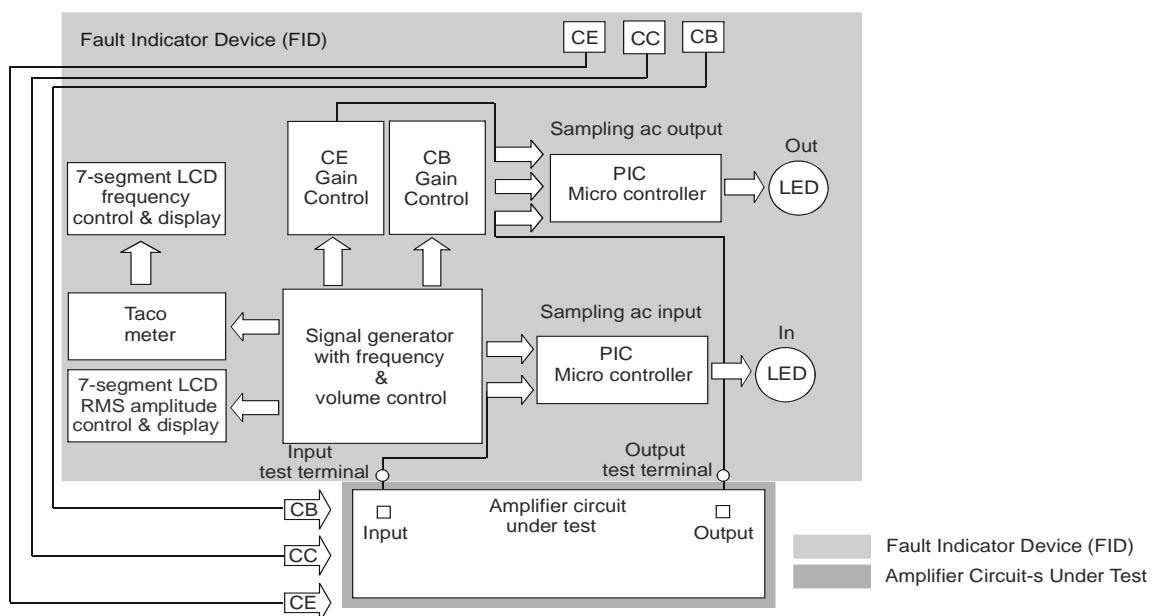


Figure 1: Block diagram of the ac input and output under test.

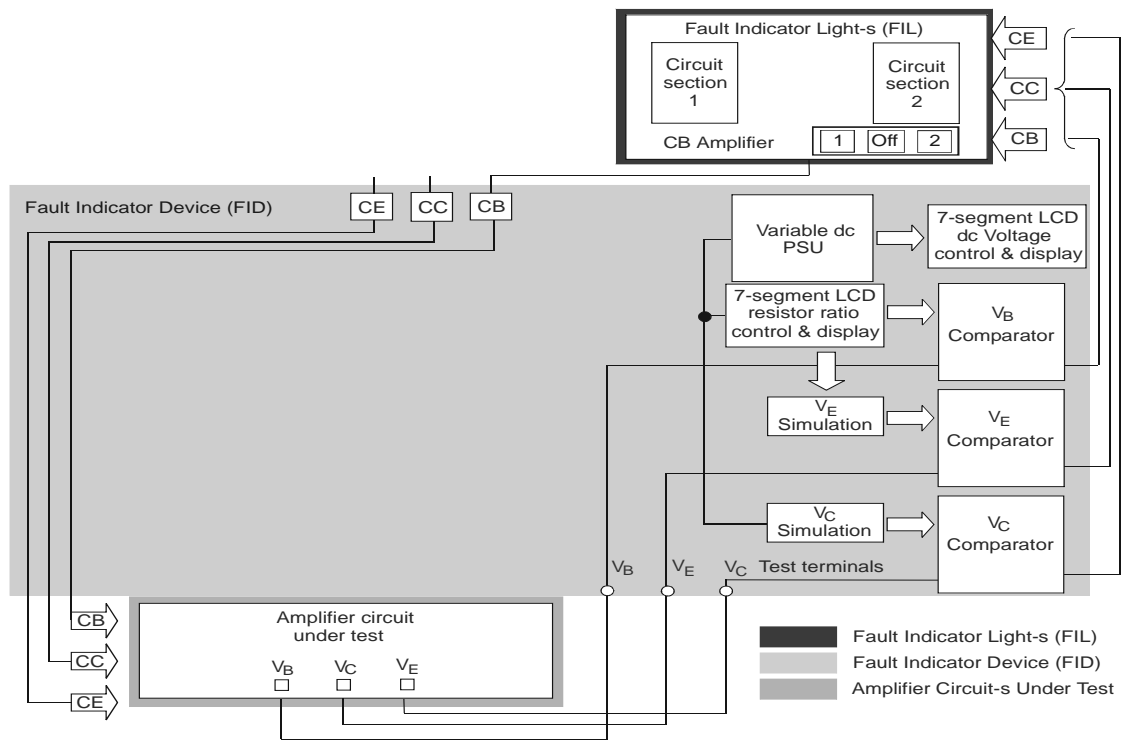


Figure 2: Block diagram of transistor dc terminals under test.

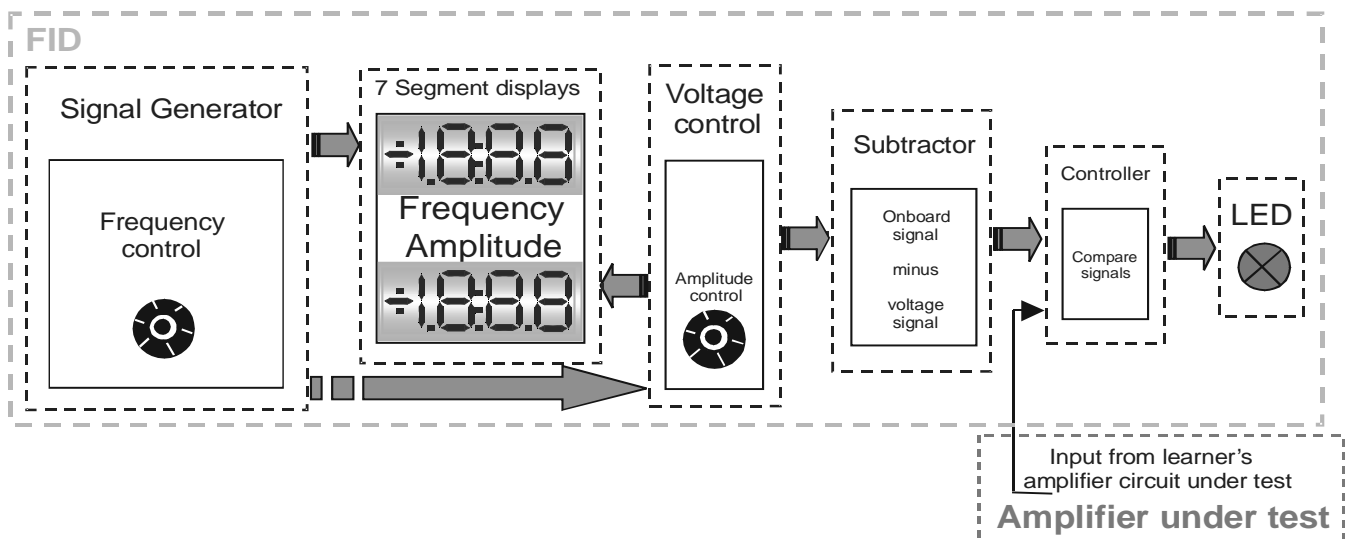


Figure 3: Block diagram of the input design layout.

## THE OUTPUT DESIGN LAYOUT

To compare the output from the amplifier circuit under test with the onboard FID signal, a voltage gain control has to be designed. The learner has to calculate the gain of the amplifier to correlate the circuit's amplified signal with the FID signal. The FID onboard gain selector can now be set to the desired value. Gain calculations should not be a problem, as it is a mathematical procedure already covered within the theory lessons.

The FID is designed to test three types of amplifier circuits, namely the common emitter (CE), the common base (CB) and the common collector (CC). It is important that there is a three-way selector onboard the FID to select the specific type of amplifier circuit being tested. Learners have to select the correct settings for the desired amplifier circuit.

There are two voltage gain selectors available on the FID. One will select the gain for the CE amplifier, while another one will determine the gain for the CB amplifier. This is necessary, as the FID onboard output signal for the CE amplifier correlation has to be  $180^\circ$  out of phase with the FID onboard supplied ac input signal. The gain selector output is the controller's input. The amplified output signal of the amplifier is also applied to the controller for correlation with the onboard signal. The output of the controller switches the output LED on when the learner's applied output signal is correct (see Figure 4).

If the output LED is off, the circuit does not deliver the correct amplification, or the gain control, on the FID, is adjusted to the wrong setting. The learner must verify the gain calculations before examining the circuit. Once the learner is sure that the gain selector has been adjusted correctly, it is safe to assume that there is something wrong with the amplifier circuit.

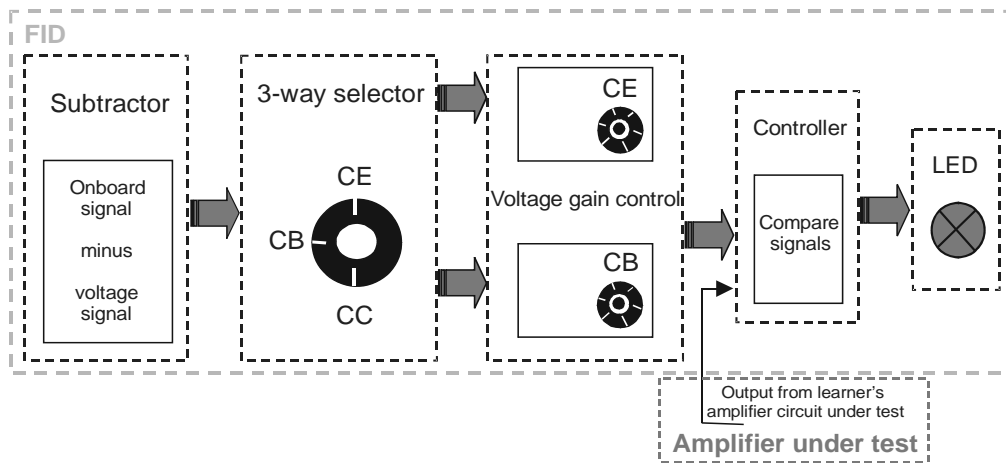


Figure 4: Block diagram of the input design layout.

### THE DC VOLTAGES DESIGN LAYOUT

It is unlikely that the construction of the amplifier circuit being tested is faulty if the transistor terminals and dc voltages test correctly. Tests conducted (regarding the dc terminal voltages) on the amplifier circuits determine the specific selected fault areas. These selected areas will correlate with the LEDs on the FIL interchangeable panels. Each type of amplifier circuit being tested has its own FIL panel.

#### The Base Voltage ( $V_B$ ) Design Layout

Comparing the circuit's base voltage with the base voltage supplied on the FID is somewhat tricky. The fact that any ratio relation of the voltage divider bias resistors, as well as any dc supply voltage ( $V_{CC}$ ), can be used for the circuit has to be taken into consideration. Therefore, it is necessary to create a similar voltage divider set-up and variable dc supply on the FID. A variable dc supply is utilised for the learner to select the same dc voltage (simulating  $V_{CC}$ ) onboard, as used in the circuit, for correlation purposes. The two base voltages are now compared via a subtractor and, should a difference occur, an LED on the FIL panel switches on, indicating a fault within a certain section of the amplifier circuit being tested. This is illustrated in Figure 5.

#### The Emitter Voltage ( $V_E$ ) Design Layout

The base-emitter junction of 0.7 V for a silicon transistor is most commonly used. Years of industrial experience within

faultfinding have proven this theory correct. The emitter voltage is 0.7 V less than the base voltage.

In order to get this voltage simulated onboard the FID, for correlation purposes, the same concept used for the base voltage can be applied. The only difference is a diode that has been added in this series to the input of the subtractor to simulate the 0.7 V drop across the base-emitter junction. This voltage is compared to the emitter voltage of the circuit being tested (see Figure 6).

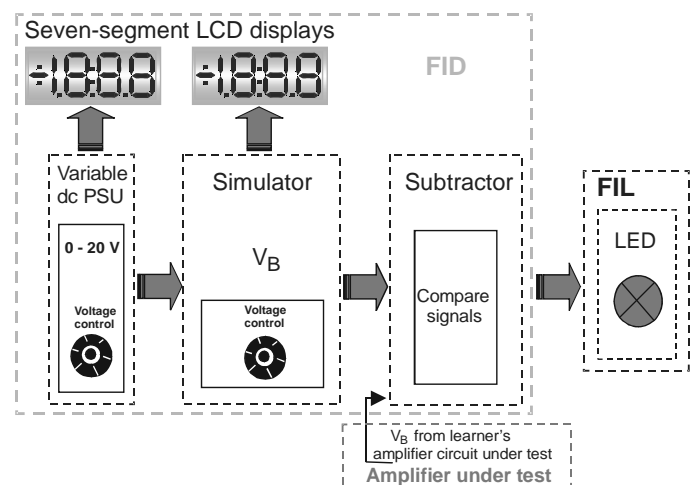


Figure 5: Block diagram of the base voltage design layout.

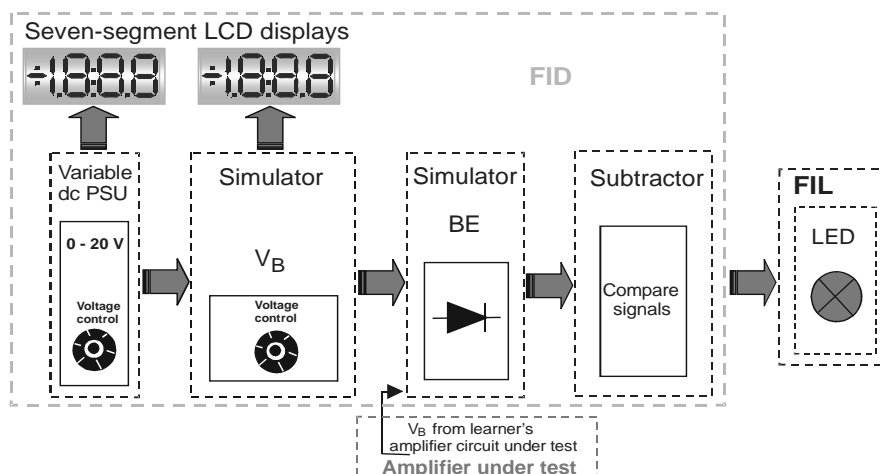


Figure 6: Block diagram of the emitter voltage design layout.

## The Collector Voltage ( $V_C$ ) Design Layout

The design for the collector voltage correlation utilises the general design rules for amplifier circuits. Designing collector voltages for an amplifier circuit takes into consideration the fact that two-thirds of the supplied dc bias voltage,  $\left(\frac{2}{3}\right)V_{CC}$ ,

needs to fall across the collector of the transistor (voltage with respect to ground), for the amplifier to operate most effectively. The onboard FID collector voltage is simulated, as  $\left(\frac{2}{3}\right)V_{CC}$ , and this is the onboard input to the subtractor circuit.

This voltage is compared with the collector voltage of the circuit under test. This is shown in Figure 7.

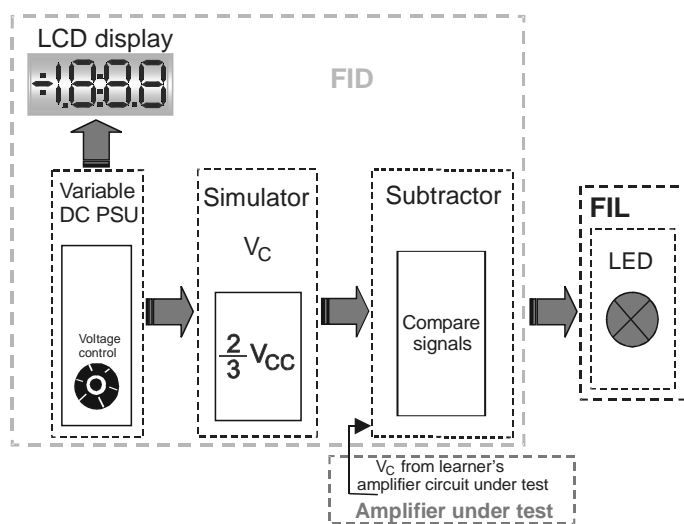


Figure 7: Block diagram of the collector design layout.

## RESULTS AND FINDINGS

The final output frequency of the onboard signal generator is limited to between 80 Hz and 2 kHz, well within the testing range of amplifier circuits. Amplifier circuits make use of a 1 kHz frequency for testing purposes. The frequency is displayed on one LCD, via a designed tachometer circuit, and has a control selector for variation purposes.

The final output voltage of the onboard signal generator is limited to  $5 V_{rms}$ , to correspond with the PIC micro-controller. The voltage is displayed on one LCD and has a control selector for variation purposes. The PIC 16F874 micro-controller is used for all three-circuit types being tested. Each controller uses the exact same software program, but differs in hardware configuration. The final output stage of the onboard signal generator is the first input into the PIC micro-controller. The PIC micro-controller samples the ac signals, comparing voltages, phase differences and frequency to correlate the ac signals with each other. If a difference of  $\pm 20\%$  occurs, the input/output LED does not light up, indicating a faulty condition.

The common emitter gain circuit emits  $180^\circ$  out of phase, which is needed between the input and output waveforms. The gain control allows the same gain setting as used within the amplifier circuit. The maximum gain allowed for this design is 50. The input and output of a common base and collector are in phase with each other. The gain for a common collector circuit is always one and no gain circuit is needed. The designed

common base gain circuit delivers the in-phase relationship needed between the input and output waveforms. The gain control allows the same gain setting as used in the amplifier circuit. The output of the gain selector is the first input to the specified PIC micro-controller. The maximum gain allowed for the common base circuit is 100.

During the dc testing phase, all ac must be removed from the circuit; therefore, the external signal generator applied to the input must be switched off to prevent the super-positioning of ac and dc signals. The power supply is set to the same dc value  $V_{CC}$  of the circuit under test. The output of the onboard power supply varies between zero and 20 V. This voltage is displayed on one LCD and has a control selector for variation purposes. A control selector for current limits is also available and is confined from 40 mA to 450 mA.

The onboard-generated base voltage is displayed on one LCD and has a control selector for variation purposes. There are three FIL panels, one for each type of amplifier circuit being tested. They are interchangeable and easily plug into the FID to identify a specific area at fault. The panels are constructed from milky Perspex with only the glow of the LEDs visible. If there is no fault in the circuit, no LED glows in the FIL panel and the circuit is in perfect working order.

Two efficiency tests were completed to test if the FID can identify faulty sections accurately. The first test was completed during fault simulation. Section selections are identified and only two variations occurred. This test proves the efficiency of the FID to be 82%. A second test occurred when an independent circuit was tested. All faulty areas were correctly specified and specific faultfinding executions took minutes to complete. This test proved the efficiency of the FID to be 100%.

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## ***3<sup>rd</sup> Global Congress on Engineering Education: Congress Proceedings***

edited by Zenon J. Pudlowski

This volume of Congress Proceedings is comprised of papers submitted for the *3<sup>rd</sup> Global Congress on Engineering Education*, which was held at Glasgow Caledonian University (GCU), Glasgow, Scotland, UK, between 30 June and 5 July 2002. The prime objective of this Congress was to bring together educators, professional organisations and industry leaders from around the world to continue discussions covering important issues, problems and challenges in engineering and technology education for this new millennium.

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